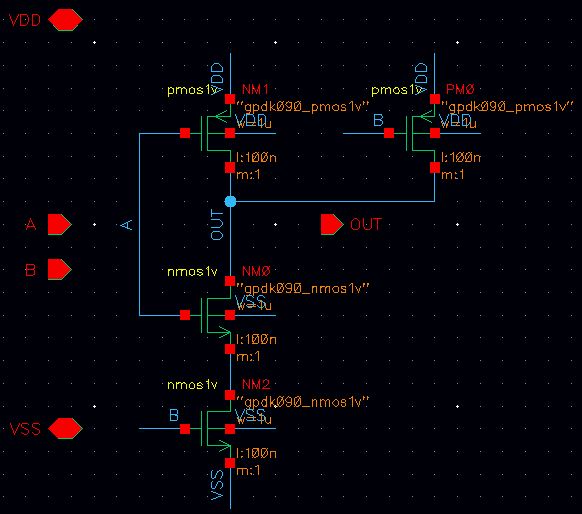
**Layout (NAND)**

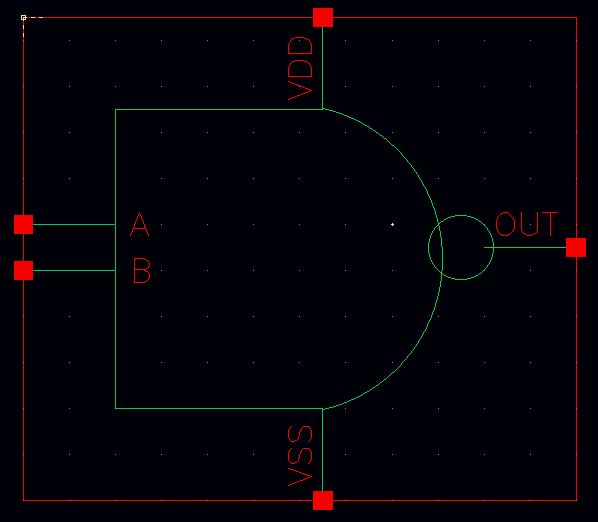
김호윤

1. Schematic

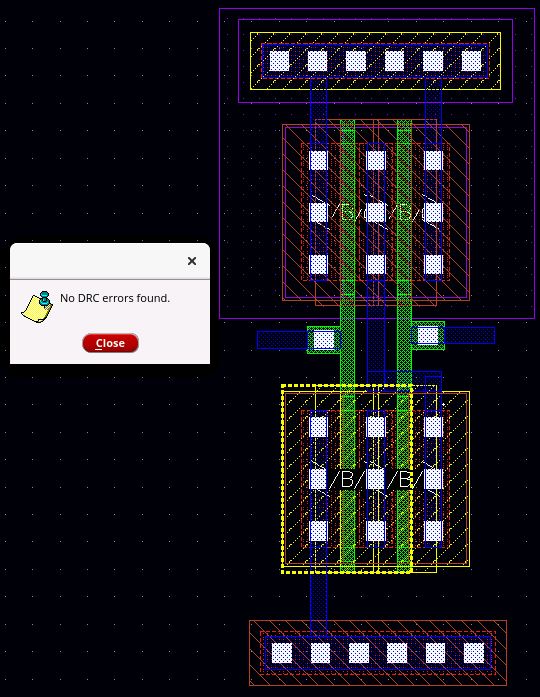


NMOS, PMOS 모두 width가 1um인 2 input NAND.

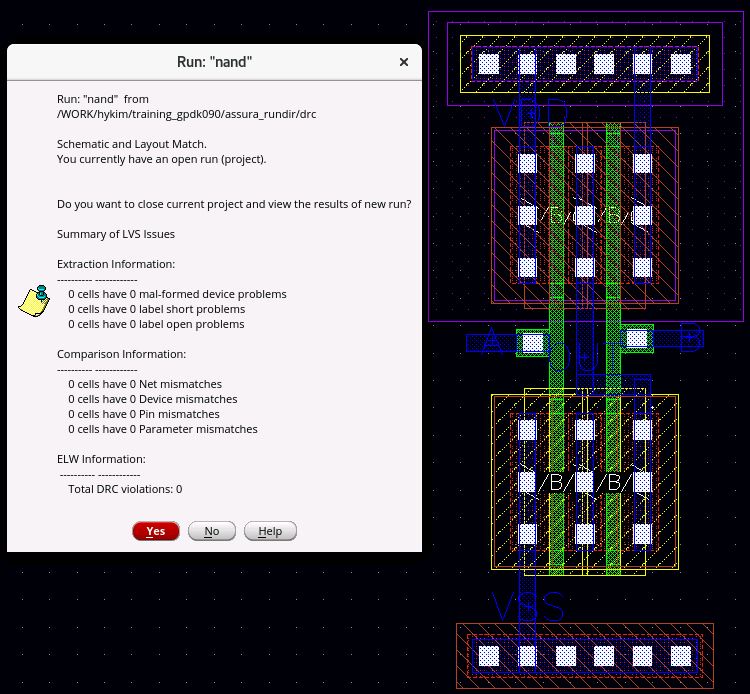
2. Symbol



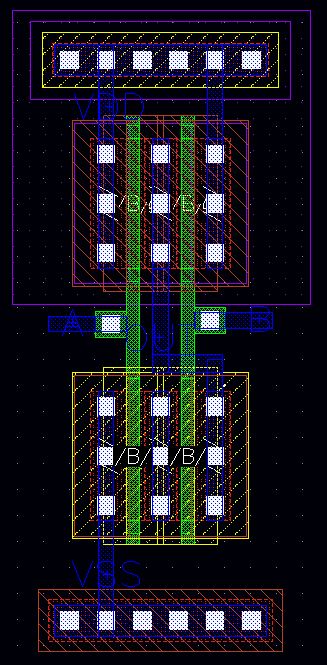
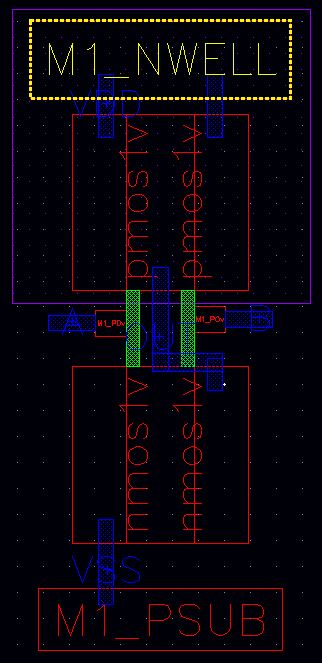
3. Layout DRC



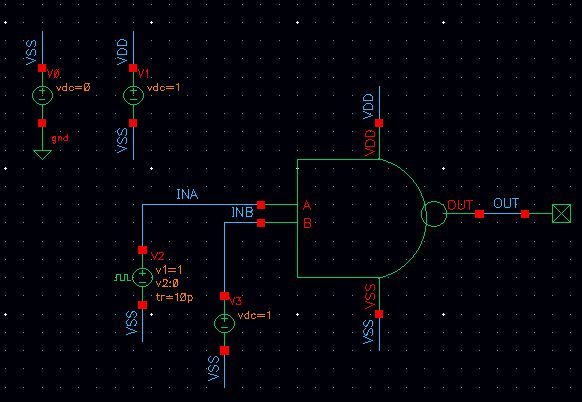
4. Layout LVS



5. Layout

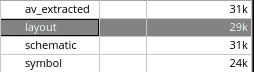
 

6. Test bench-NAND



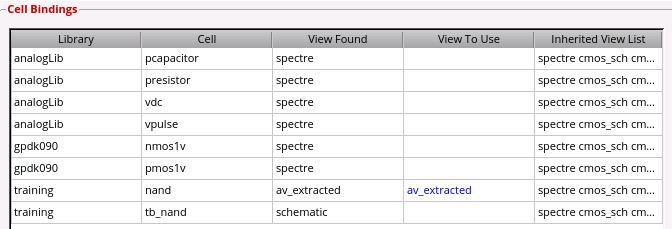
Input A에 period 100ps, rising/falling time 10ps인 신호를 인가. Input B는 1V dc 신호 인가.

7. Post-layout simulation



Layout에서 assura - run quantus를 실행하여 extraction type: RC, cap coupled가 되도록 설정을 하고 extraction 진행. 위 그림은 nand cell에 av\_extracted가 생성된 모습이다.

Post-layout simulation을 하기 위해 우선 테스트벤치에 config view를 생성하고 아래와 같이extracted netlist가 config view에 포함이 되도록 설정한다.



ADE를 이용하여 setup - design에서 tb\_nand를 schematic과 config를 각각 선택하여 총 두번의 시뮬레이션을 진행하면 아래와 같은 결과가 나온다.

